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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/724,989

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Visvesvaraya A. Pentakota

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07/18/2006

TEXAS INSTRUMENTS INCORPORATED

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EXAMINER

TON, MY TRANG

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/724,989

Applicant(s)

PENTAKOTA ET AL.

Examiner

My-Trang N. Ton

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 24 April 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 6,7,10,11,18,19,22 and 23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6,7,18 and 19 is/are allowed.
- 6) ☒ Claim(s) 10,11,22 and 23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.


## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

  
MY-TRANG NUTON  
PRIMARY EXAMINER

## Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

The Amendment filed on 4/24/06 has been received and entered in the case. In view of newly discovered prior art, new ground of rejection are now set forth. Any inconvenience caused by the delay in citing this new prior art is regretted. In view of the new grounds of rejection not necessitated by Applicants Amendments, this action is non-final.

***Claim Rejections - 35 USC § 103***

Claims 10-11, 22-23 remain rejected under 35 U.S.C 102(3) as being unpatentable over Flannagan (U.S Patent No. 6,031,408) and further in view of Li (U.S Patent No. 6,836,160) for the reasons recited in the last Office action.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 10-11 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beeman (U.S Patent No. 6,614,284).

Beeman discloses in figs. 1 and 5 a circuit including:

a first transistor (Q21) designed to be turned on when a voltage level is outside of the specified range;

a current amplifier (Q22, Q23) drawing a current from a node (N21) when the first transistor (Q21) is turned on, which causes said voltage level at the node (N21) to be pulled to within the specified range;

a biasing circuit (102) generating a bias signal (Vin) to a gate terminal of the first transistor (Q21), wherein a voltage level of the bias signal (Vin) is determined by an upper limit (High) or a lower limit (Low) of the specified range; and

wherein the current amplifier (Q22, Q23) includes: a second transistor (Q22), a third transistor (Q23) and a resistor (R52).

However, this reference does not specifically shown "a gate, a drain, a source" as recited in claim 10, "the second transistor and the third transistor comprises a NMOS transistor" as recited in claim 11.

Nevertheless, field effect transistors (having the gate, the drain, the source) are well-known switching devices and patentable equivalent to bipolar transistors (Q21-Q23) since no unobvious results are seen produce from their use. Therefore, it would have been obvious at the time of the invention was made for one skilled in the art to utilize these particular types of transistors because of this well-known advantages in performance and integration. FETs have very short switching times and very low electrical power consumption.

It is noted that patentability may not be based on the mere labeling of the name of the clamping circuit. That is, the name, constitutes non-patentable subject matter. With the same structure in Beeman, ostensibly the same function (clamping) is achieved.

Claims 22-23 are similarly rejected as claims 10-11.

Claims 10-11, 22 and 23 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Flannagan (U.S Patent No. 6,031,408) and further in view of Kimura (U.S. Patent No. 5,990,727).

Flannagan discloses in Fig. 6 a square low clamping circuit including:

Regarding claim 10:

a first transistor (132) designed to be turned on when the voltage level is outside of the specified range (when 132 ON); and

a current amplifier (135 and 136) drawing a substantial amount of current from the node (121) when the first transistor is turned on (132 ON), which causes the voltage level at the node (121) to be pulled to within the specified range;

biasing circuit (130, 131, 133, 134) generating a bias signal to a gate terminal of the first transistor (132), wherein a voltage level of the bias signal is determined by an upper limit or a lower limit of the specified range,

wherein the current amplifier (135, 136) comprises:

a second transistor (135) and a third transistor (136), wherein a gate terminal of the third transistor (136) is connected to both drain and gate terminals of the second transistor (135), a source terminal of the third transistor (136) is connected to ground (Vss), the drain terminal of the second transistor (135) is connected to a drain terminal of the first transistor (132), and a drain terminal of the third transistor (136) is connected to a source terminal of the first transistor (132).

Art Unit: 2816

However, this reference does not specifically disclose "a resistor connected between a source terminal of said second transistor and ground" as recited in claim 10.

Kimura teaches in Fig. 5 a well-known feature in the art for providing higher resistance, more voltage drop and increasing the impedance in the circuit by having the source of M1 is grounded through the resistor R1.

Therefore, it would have been obvious at the time the invention was made for one skilled in the art to use the teaching as taught in Kimura for the Flannagan's reference by inserting the resistor between a source terminal of the second transistor (135) and ground (Vss) for the purpose of providing more voltage drop, higher resistance and increasing the impedance.

Regarding the limitation of claim 11: each of the second transistor and the third transistor comprises a NMOS transistor (135-136).

Claims 22-23 are similarly rejected as claims 10-11.

#### ***Allowable Subject Matter***

Claims 6-7 and 18-19 are allowable over the prior art of record.

#### ***Response to Arguments***

Applicant's arguments filed 4/24/06 have been fully considered but they are not persuasive. Examiner has thoroughly reviewed Applicant's arguments but firmly believes that the cited references reasonably and properly meet the claimed limitation as rejected.

Art Unit: 2816

Applicant's argument – Li does not teach or suggest the addition of such resistor in such a clamping circuit or Li does not disclose a clamping circuit and does not use a current mirror in a closed feedback loop configuration.

Examiner's response - The argument regarding Li fails to disclose "the addition of such resistor in such a clamping circuit " or "Li does not use a current mirror in a closed feedback loop configuration" is not relevant since Flannagan (Fig. 6) teaches such limitation as pointed out in the last Office action. Li was cited simply to teach the use of a well-known feature: resistor connected between a source terminal and a ground in the current mirror circuit arrangement. The skilled artisan would have been motivated to employ the resistor between the source terminal of transistor 135 and the ground of the Flannagan's reference for the purpose of providing higher resistance. Moreover, it is noted patentability may not be based on the mere labeling of the name of the circuit (i.e., clamping circuit). That is, the name, constitutes non-patentable subject matter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



My-Trang N. Ton  
Primary Examiner  
Art Unit 2816

July 10, 2006